Amendments to the Claims

1. (CURRENTLY AMENDED) An oscillator circuit for generating a high-frequency electromagnetic oscillation, comprising:

- an amplifier configuration with at least one input and at least one output,
- an oscillator crystal connected to at least one of the outputs of the amplifier configuration,
- a bandpass filter configuration, which is connected, with at least one input, to the oscillator crystal and the at least one output of the amplifier configuration connected to the oscillator crystal, and back coupled, with at least one output, to the input, or at least one of the inputs, of the amplifier configuration,

wherein, through dimensioning of the amplitude-frequency characteristic and/or the phase-frequency characteristic of the bandpass filter configuration as a function of the amplitude-frequency characteristic and the phase-frequency characteristic of the amplifier configuration and the oscillator crystal, the oscillation condition is fulfilled exclusively for a selected harmonic of the oscillator crystal, and the high-frequency, electromagnetic oscillation formed by this selected harmonic of the oscillator crystal is available at the output of the bandpass filter configuration.

2. (ORIGINAL) An oscillator circuit as claimed in claim 1, characterized in that the amplifier configuration is designed with, in each case, at least one pair of at least substantially symmetrical inputs and outputs (differential inputs and outputs) for processing electromagnetic oscillations (known as differential signals), operated at least substantially symmetrically relative to a first reference potential.

3. (ORIGINAL) An oscillator circuit as claimed in claim 2, characterized in that the amplifier configuration comprises a differential amplifier circuit, which is equipped with two field effect transistors coupled at their source terminals, the gate terminals of which are each coupled with one of the differential inputs of the amplifier configuration, wherein a drain terminal of each field effect transistor forms one of the differential outputs of the amplifier configuration, each of which is further coupled,

via a load path, which comprises at least one field effect transistor, designated an output load transistor, with a terminal carrying a second reference potential.

4. (ORIGINAL) An oscillator circuit as claimed in claim 3, characterized in that the amplifier configuration comprises a control-voltage generation stage for generating a control voltage, which is supplied to gate terminals of the output load transistors.

5. (ORIGINAL) An oscillator circuit as claimed in claim 4, characterized in that the control-voltage generation stage comprises a series circuit comprising a constant current source and a field effect transistor bridged between its drain terminal and gate terminal.

6. (ORIGINAL) An oscillator circuit as claimed in claim 5, characterized in that the amplifier configuration comprises an operating-point regulating stage with three field effect transistors, a first of which is disposed in the first load path and a second of which is disposed in the second load path, each connected in series with the output load transistor there, and a third of which is connected in series with the series circuit comprising the constant current source and field effect transistor of the control-voltage generation stage, wherein a gate terminal of the first of the three field effect transistors of the operating-point regulating stage is connected to a first of the differential outputs of the amplifier configuration, wherein a gate terminal of the second of the three field effect transistors of the operating-point regulating stage is connected to a second of the differential outputs of the amplifier configuration, wherein a gate terminal of the third of the three field effect transistors of the operating-point regulating stage is connected to the gate terminals of the output load transistors and wherein the three field effect transistors of the operating-point regulating stage are routed, with their source terminals, to the terminal carrying the second reference potential.

7. (CURRENTLY AMENDED) An oscillator circuit as claimed in claim 3, characterized in that the amplifier configuration comprises an offset compensation device comprising, in each case, a high-pass circuit between:

- each of the differential inputs of the amplifier configuration,
- the gate terminal of the field effect transistor of the differential amplifier circuit comprising the amplifier configuration that is coupled with this differential input,
- the differential output formed by the drain terminal of said field effect transistor,

wherein the limiting frequency is small as compared with the frequency operating range of the oscillator circuit.

8. (ORIGINAL) An oscillator circuit as claimed in claim 7, characterized in that each of the high-pass circuits contains a capacitor, via which the differential input of the amplifier configuration is coupled with the gate terminal of the field effect transistor of the differential amplifier circuit comprising the amplifier configuration, and each of the high-pass circuits further contains an ohmic resistance element, via which the gate terminal of the field effect transistor of the differential amplifier circuit comprising the amplifier configuration is coupled with the differential output of the amplifier configuration formed by the drain terminal of the field effect transistor.

9. (ORIGINAL) An oscillator circuit as claimed in claim 3, characterized in that the amplifier configuration is coupled with an auxiliary starting circuit, by means of which, during a predetermined period when the oscillator circuit is put into operation, a differential voltage is supplied to the gate terminals of the field effect transistors, coupled at their source terminals, of the differential amplifier circuit comprising the amplifier configuration.

10. (CURRENTLY AMENDED) An oscillator circuit as claimed in claim 9, characterized in that the auxiliary starting circuit preferably comprises:

- a first field effect transistor, which is disposed between the gate terminal of a first of the field effect transistors, coupled at their source terminals, of the differential amplifier circuit comprising the amplifier configuration, and a third reference potential;
- a second field effect transistor, which is disposed between the gate terminal of a second of the field effect transistors, coupled with their source terminals, of the differential amplifier circuit comprising the amplifier configuration, and the third reference potential;
- a start-signal input for supplying an at least largely pulse-shaped or step-shaped start signal when the oscillator circuit is put into operation;
- a delay stage;

wherein the start-signal input is directly coupled with a gate terminal of the first field effect transistor of the auxiliary starting circuit and, via the delay stage, with a gate terminal of the second field effect transistor of the auxiliary starting circuit.

11. (ORIGINAL) An oscillator circuit as claimed in claim 2, characterized in that the oscillator crystal takes the form of a two-terminal network and is connected with, in each case, one of its terminals to, in each case, one of the outputs of a pair of differential outputs of the amplifier configuration, in order to supply an electromagnetic oscillation emitted by the amplifier configuration in the form of a differential signal

12. (ORIGINAL) An oscillator circuit as claimed in claim 1, characterized in that the bandpass filter configuration is designed with, in each case, at least one pair of at least virtually symmetrical input and outputs (known as differential inputs and outputs) for processing electromagnetic oscillations (known as differential signals), operated at least virtually symmetrically relative to a fourth reference potential.

13. (ORIGINAL) An oscillator circuit as claimed in claim 12, characterized in that the bandpass filter configuration is connected, with at least one pair of its differential inputs, to at least the pair of differential outputs of the amplifier configuration that are connected to the terminals of the oscillator crystal, and, with at least one pair of its differential outputs, to at least one pair of differential inputs of the amplifier configuration.

14. (ORIGINAL) An oscillator circuit as claimed in claim 13, characterized in that the bandpass filter configuration is designed with a cascade connection of at least two bandpass stages of low quality.

15. (ORIGINAL) An oscillator circuit as claimed in claim 14, characterized in that the bandpass stages are designed, each with a differential amplifier circuit having two field effect transistors coupled at their source terminals, and with one pair of differential inputs and one pair of differential outputs, wherein each one of the differential inputs is coupled, via one of the high-pass circuits, with one of the gate terminals of one of the field effect transistors, and each one of the drain terminals of the field effect transistors forms one of the differential outputs of the bandpass stages, each of which drain terminal is further connected, via one of the low-pass circuits, to a terminal carrying a fifth reference potential, wherein the differential inputs of a first of the bandpass stages disposed in a cascade connection form the differential inputs of the bandpass filter configuration that are connected to the terminals of the oscillator crystal, and wherein the differential outputs of a last of the bandpass stages disposed in a cascade connection form the differential outputs of the bandpass filter configuration that are connected to the differential inputs of the amplifier configuration.

16. (ORIGINAL) An oscillator circuit as claimed in claim 15, characterized in that the high-pass circuits and/or the low-pass circuits take the form of RC networks.

17. (ORIGINAL) An oscillator circuit as claimed in claim 16, characterized in that the RC networks are equipped with switchable ohmic resistors.

18. An oscillator circuit as claimed in claim 17, characterized by a trimming circuit to trim the resistance values of the switchable ohmic resistors in the RC networks with a reference resistor.

19. (ORIGINAL) An oscillator circuit as claimed in claim 12, characterized by a converter circuit, coupled with at least one pair of differential outputs of the bandpass filter configuration, for converting the differential signal emitted by these differential outputs into an electromagnetic oscillation operated asymmetrically relative to the fourth reference potential.

20. (CURRENTLY AMENDED) An oscillator circuit as claimed in claim 19, characterized in that the converter circuit comprises:

- an input stage designed as a differential amplifier with field effect transistors coupled at their source terminals, to which the differential signal to be converted is supplied;
- a first current mirror stage designed with field effect transistors coupled via their gate terminals, to mirror a first differential output signal of the input stage of the converter circuit into a first intermediate signal;
- a second current mirror stage designed with field effect transistors coupled via their gate terminals, to mirror a second differential output signal of the input stage of the converter circuit into a second intermediate signal;
- a third current mirror stage designed with field effect transistors coupled via their gate terminals, to mirror the first intermediate signal of the first current mirror stage of the converter circuit into a third intermediate signal;
- a subtraction circuit, designed as a current node, to subtract the second intermediate signal from the third intermediate signal;
- an output driver circuit;

wherein the third current mirror stage is further coupled with:

- an auxiliary switch-on stage with a first cascode field effect transistor in the input arm of the third current mirror stage;
- an auxiliary switch-off stage, comprising:
  - a first cascaded stage with a series circuit comprising:

- a first field effect transistor, which is incorporated into the second current mirror stage and which is operated, jointly with the second current mirror stage, by the second differential output signal of the input stage of the converter circuit, to emit a fourth intermediate signal, which is, at least over segments, essentially proportional to the second intermediate signal;
- an input transistor, designed as a field effect transistor, of a fourth current mirror stage;
- a second cascode field effect transistor in the input arm of the fourth current mirror stage;

the fourth current mirror stage to mirror the fourth intermediate signal into a fifth intermediate signal and to supply it to the third current mirror stage, comprising:

- the input transistor, designed as a field effect transistor, to supply the fourth intermediate signal;
- an output transistor, designed as a field effect transistor, to emit the fifth intermediate signal;

and wherein a cascode-bias-voltage generating circuit is provided to supply a common cascode bias voltage to gate terminals, coupled together, of the first and second cascode field effect transistors.

21. (ORIGINAL) An oscillator circuit as claimed in claim 20, characterized in that the cascode-bias-voltage generating circuit comprises a series circuit comprising a first and a second field effect transistor and a constant current source, which is disposed between a terminal carrying a sixth reference potential and a terminal carrying a seventh reference potential, wherein this first field effect transistor is connected, with its drain terminal, to a source terminal of the second field effect transistor, and gate terminals of this first and this second field effect transistor are connected to each other, to a drain terminal of the second field effect transistor and to the gate terminals of the first and the second cascode field effect transistors to supply the common cascode bias voltage.